|  |  |
| --- | --- |
| IF/ID | |
| Input port | Output port |
| instr[15:0] | instr\_IF/ID[15:0] |

|  |  |
| --- | --- |
| instr\_decoder | |
| Input port | Output port |
| instr\_IF/ID[15:0] | w1\_reg [2:0] |
| reg\_en[2:0] |
| read\_reg1 [2:0] |
| read\_reg2[2:0] |
| b\_sel |
| mem\_en |
| mem\_wr |
| write\_src[4:0] |
| ext\_16 [15:0] |
| alu\_sign |
| alu\_inv |
|  |
|  |
|  |

rf\_bypass

|  |  |
| --- | --- |
| ID/EX | |
| Input port | Output port |
| w1\_reg[2:0] | w1\_reg \_ID/EX[2:0] |
| reg\_en[2:0] | reg\_en\_ID/EX[2:0] |
| b\_sel | b\_sel\_ID/EX |
| mem\_en | mem\_en\_ID/EX |
| mem\_wr | mem\_wr\_ID/EX |
| write\_src[4:0] | write\_src\_ID/EX[4:0] |
| ext\_16[15:0] | ext\_16\_ID/EX [15:0] |
| alu\_sign | alu\_sign\_ID/EX |
| alu\_inv | alu\_inv\_ID/EX |
| rs [15:0] | rs\_ID/EX [15:0] |
| r2 [15:0] | r2\_ID/EX[15:0] |
|  |  |
|  |  |
|  |  |

alu\_s, alu\_i, alu\_bmux, sign\_extender, ALU, lt\_lte, reverse Rs, forward unit

|  |  |
| --- | --- |
| EX/MEM | |
| Input Port | Output Port |
| w1\_reg \_ID/EX[2:0] | w1\_reg \_EX/MEM[2:0] |
| reg\_en\_ID/EX[2:0] | reg\_en\_EX/MEM[2:0] |
| mem\_en\_ID/EX | mem\_en\_EX/MEM |
| mem\_wr\_ID/EX | mem\_wr\_EX/MEM |
| write\_src\_ID/EX[4:0] | write\_src\_EX/MEM[4:0] |
| alu\_out [15:0] | alu\_out\_EX/MEM [15:0] |
| r2\_ID/EX[15:0] | r2\_EX/MEM[15:0] |
| rs\_ID/EX [15:0] | rs\_EX/MEM [15:0] |
| alu\_zero | alu\_zero\_EX/MEM |
| alu\_ofl | alu\_ofl\_EX/MEM |
| Cout | Cout\_EX/MEM |
| lt | lt\_EX/MEM |
| lte | lte\_EX/MEM |
| rs\_inv[15:0] | rs\_inv[15:0]\_EX/MEM |

dmem, wrt\_ctrl,

|  |  |
| --- | --- |
| MEM/WB | |
| Input Port | Output Port |
| w1\_reg \_EX/MEM[2:0] | w1\_reg \_MEM/WB[2:0] |
| reg\_en\_EX/MEM[2:0] | reg\_en\_MEM/WB[2:0] |
| writedata [15:0] | writedata\_MEM/WB [15:0] |

Forward unit

|  |  |  |  |
| --- | --- | --- | --- |
| w1\_reg\_MEM/WB== read\_reg1  !reg\_en\_EX/MEM  w1\_reg\_EX/MEM!=read\_reg1 | w1\_reg\_MEM/WB==  read\_reg2  !reg\_en\_EX/MEM  w1\_reg\_EX/MEM!=read\_reg1 | w1\_reg\_EX/MEM= =read\_reg1  reg\_en\_EX/MEM | w1\_reg\_EX/MEM= =read\_reg2  reg\_en\_EX/MEM |
| alu\_rs=writedata\_MEM/WB | alu\_r2=writedata\_MEM/WB | alu\_rs=writedata\_EX/MEM  (need mux to select which output from EX/MEM) | alu\_r2=writedata\_EX/MEM  (need mux to select which output from EX/MEM) |